Modeling and control of serial multicellular converters by Petri Nets

- Fernando SALINAS
- Malek GHANES
- Jean-Pierre BARBOT
- Miguel F. Escalante

UANL, FIME-Lab DIE, Av. Universidad S/N, CP 66460, San Nicolás de los Garza, México
ECS-Lab 3649 EA ENSEA, 6 avenue du Ponceau 95014, Cergy-Pontoise Cedex, France

Outline

- Introduction
- Objectives
- Description
- Simulation results
- Experimental results
- Conclusion

Introduction

Power electronics. Control and conditioning the electric energy using solid and states devices.

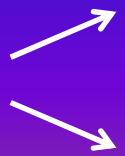
Serial Multicellular Converter (SMC). T. A. Meynard and H. **Foch**.
Power Electronics Specialists Conference, 1992

Advantages of SMC

- Synthesize a high voltage signal using low-voltage semiconductor components
- The voltage gradient of the output waveform is decreased. There exist an increase in the lifetime of the dielectrics of the equipment
- Inverter configuration. The output waveform has a low harmonic distortion and if the number of levels is sufficiently high, the filtering stage can be eliminated.

Disadvantage of SMC

- Unbalanced in the capacitor voltages

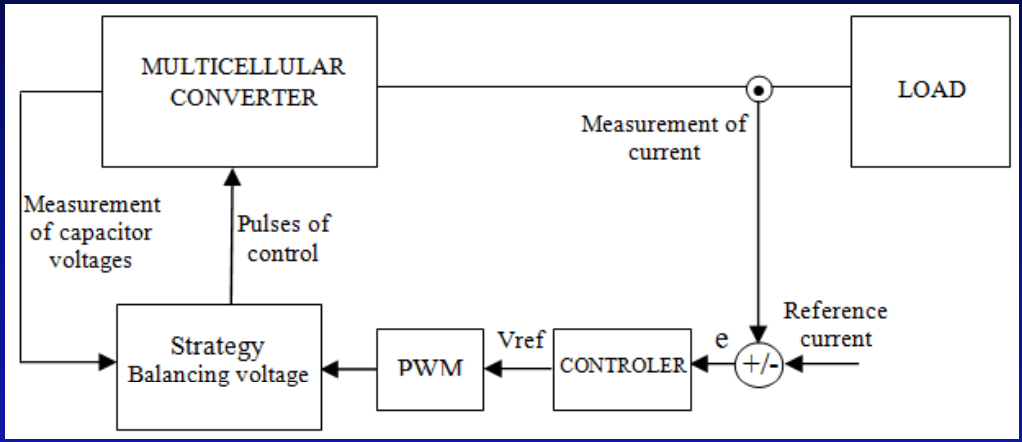


Natural balance

Active balance

Note: Both structures require a current control regardless of application

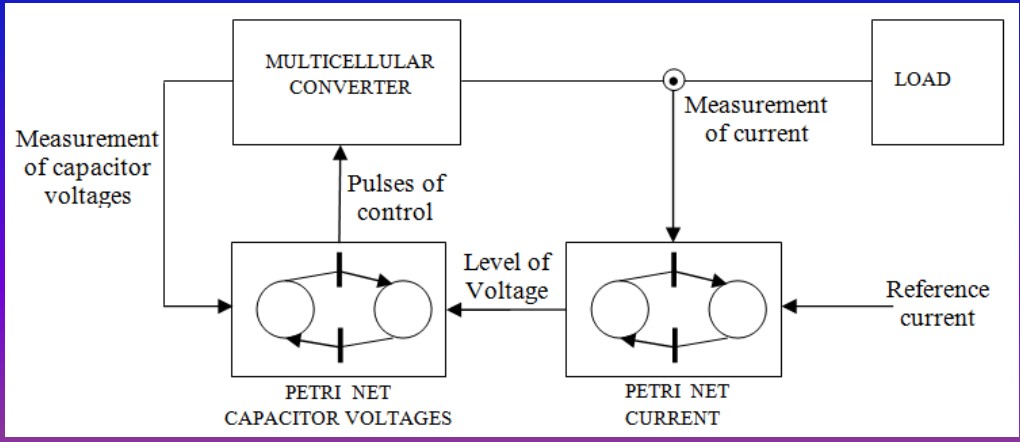
Introduction



← Common structure of control

- General objective

Incorporate the "Petri Nets approach," as a design tool of control techniques, in power electronics systems.



← Proposed structure of control

- Particular objectives
  - Ensure the demanded reference of current.
  - Ensure the balancing of capacitor voltages.

System modeling and description

Basic 4-level SMC

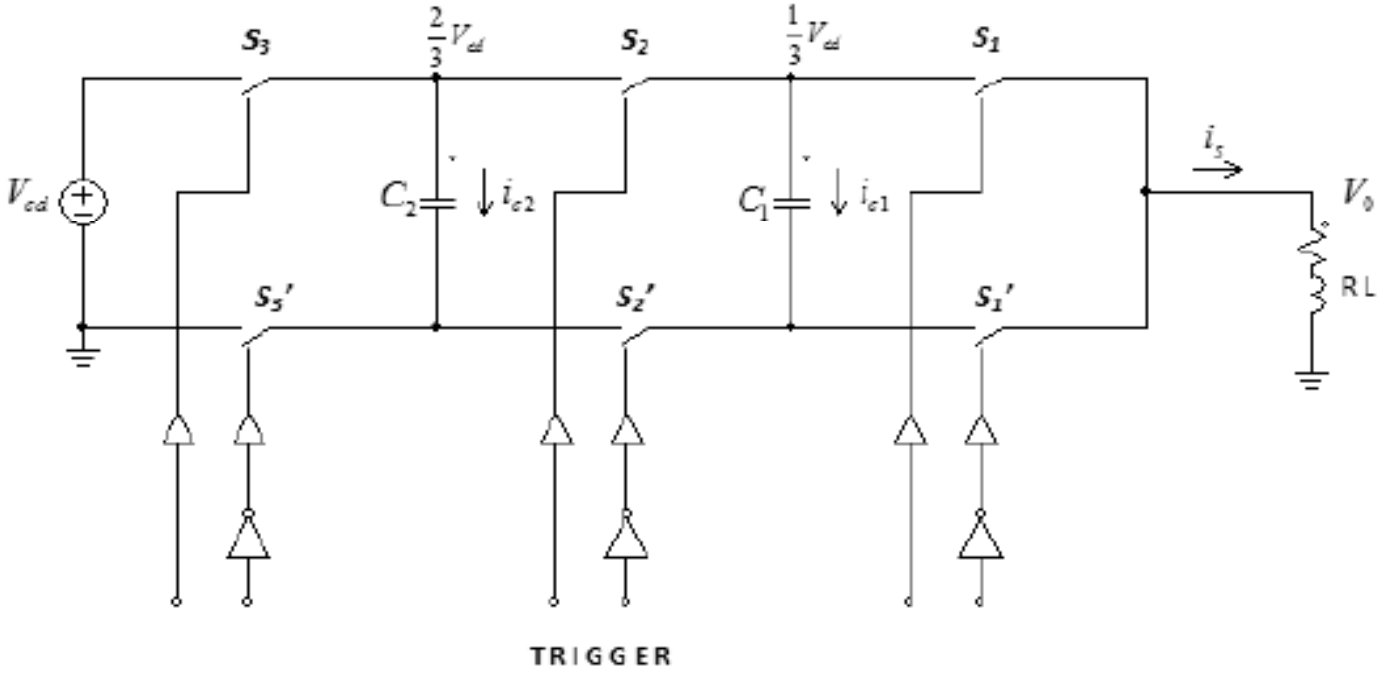
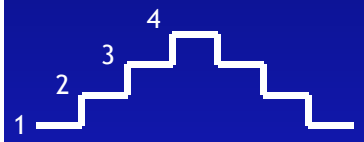


Figure1. Four level multicellular converter



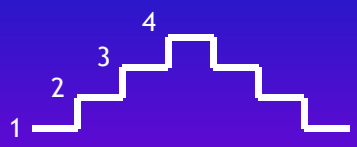
Multilevel
Output voltage

System modeling and description

Effect of switching states on internal variables

Level	Command pulses			Assignation	is toward load		is toward converter	
	S3	S2	S1		Vc2	Vc1	Vc2	Vc1
1	0	0	0	q0	-	-	-	-
2	0	0	1	q1	-	0	-	1
	0	1	0	q2	0	1	1	0
	1	0	0	q4	1	-	0	-
3	0	1	1	q3	0	-	1	-
	1	0	1	q5	1	0	0	1
	1	1	0	q6	-	1	-	0
4	1	1	1	q7	-	-	-	-

s_k Switching States :
(1) on, (0)off
i_s Current direction
Vc_k Capacitor condition :
(1) charging mode
(0) discharging mode
(–) Not change



Multilevel
Output voltage

System modeling and description

The converter model can be expressed as follows:

$$V_0 = \sum_{k=1}^{p} (v_{Ck} - v_{C(k-1)}) \cdot sc_k$$

$$i_{ck} = \left(sc_{(k+1)} - sc_k \right) \cdot i_S$$

$$v_{sk} = \left(v_{Ck} - v_{C(k-1)} \right) \cdot sc_k$$

$$v_{sk}' = (v_{Ck} - v_{C(k-1)}) \cdot \overline{sc_k}$$

$$sc_k = \begin{cases} 1 \ if \ \ S_k \ is \ on \ \ for \ \ k = 1,.., p \\ 0 \ if \ \ S_k \ is \ off \ \ \ for \ \ k = 1,.., p \end{cases}$$

$$v_{Ck} = \frac{k}{p} V_{cd} \ for \ k = 1,....p-1$$

$$\Delta v_{Ck} = \frac{1}{C_k} \int_{t1}^{t2} i_{ck} \cdot dt \approx 0$$

System modeling and description

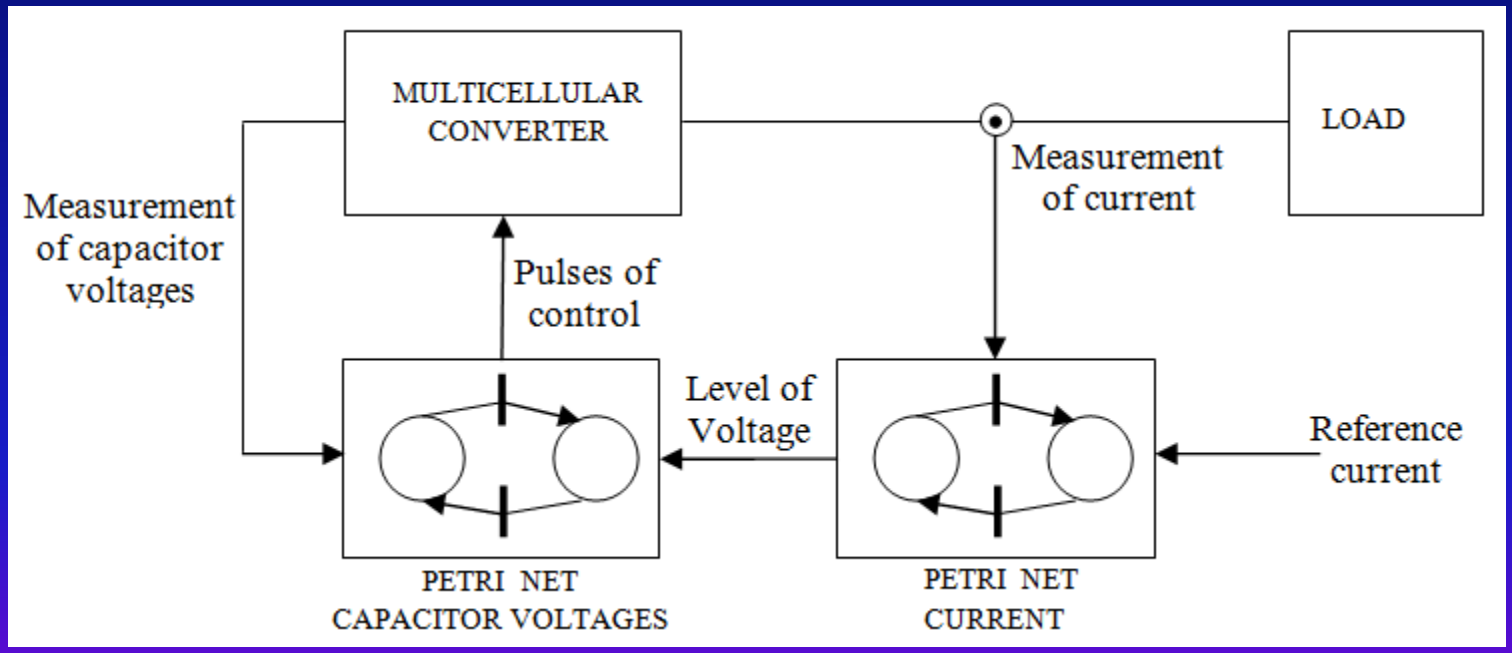
The converter model can be expressed as follows:

$$\dot{x}(t) = f(S_k, x(t)) = A(S_k) \cdot x(t) + b(S_p) \cdot u$$

$$\begin{bmatrix} \dot{i}_L \\ \dot{V}_{c_1} \\ \dot{V}_{c_2} \\ \vdots \\ \dot{V}_{c_{p-1}} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & (S_1 - S_2)\frac{1}{L} & (S_2 - S_3)\frac{1}{L} & \cdots & (S_{p-1} - S_p)\frac{1}{L} \\ (S_2 - S_1)\frac{1}{C_1} & 0 & \cdots & \cdots & 0 \\ (S_3 - S_2)\frac{1}{C_2} & \vdots & \ddots & & \vdots \\ \vdots & \vdots & & \ddots & \vdots \\ (S_p - S_{p-1})\frac{1}{C_p} & 0 & \cdots & \cdots & 0 \end{bmatrix} \begin{bmatrix} i_L \\ V_{c_1} \\ V_{c_2} \\ \vdots \\ V_{c_p} \end{bmatrix} + \begin{bmatrix} \frac{V_{cd}}{L} \cdot S_p \\ 0 \\ \vdots \\ \vdots \\ 0 \end{bmatrix}$$

Hybrid control by Petri Nets

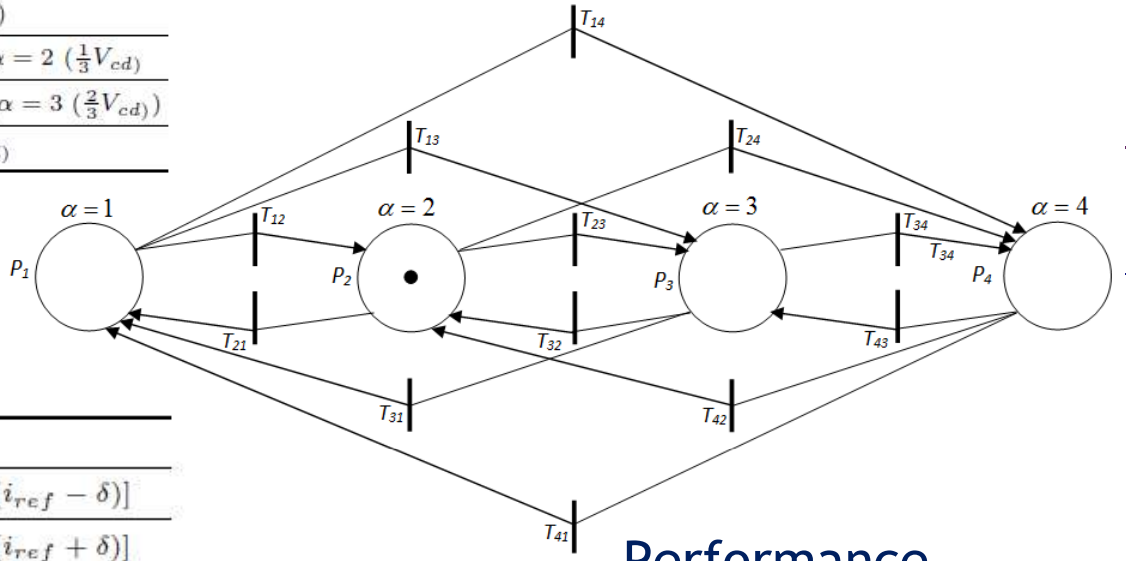
Hybrid control by Petri Nets proposed in the multicellular converter



Hybrid control by Petri Nets

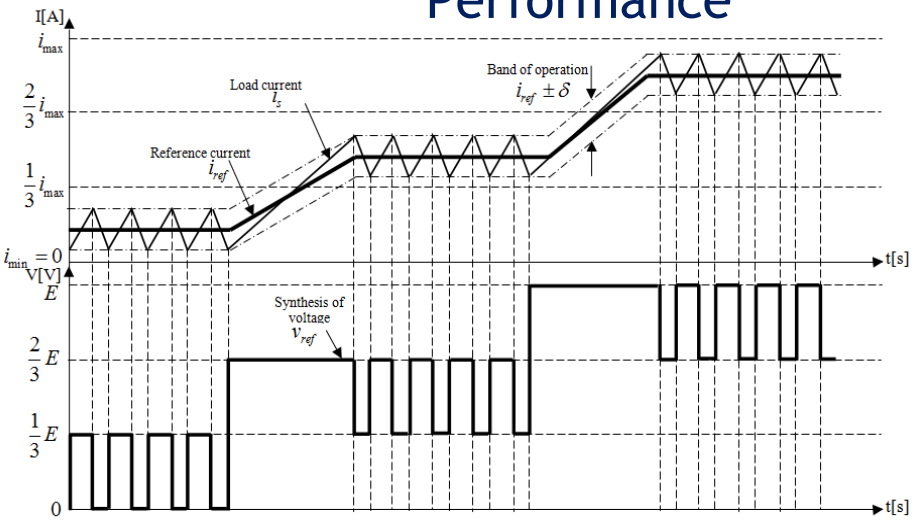
Places	Designations
P_1	Level of voltage minimum in SMC, $\alpha = 1$ $(0V)$
P_2	A third of the maximum voltage level available in SMC, $\alpha = 2$ $(\frac{1}{3}V_{cd})$
P_3	Two thirds of the maximum voltage level available in SMC,$\alpha = 3$ $(\frac{2}{3}V_{cd})$
P_4	Level of voltage maximum in SMC, $\alpha = 4$ (V_{cd})

Petri Net of current



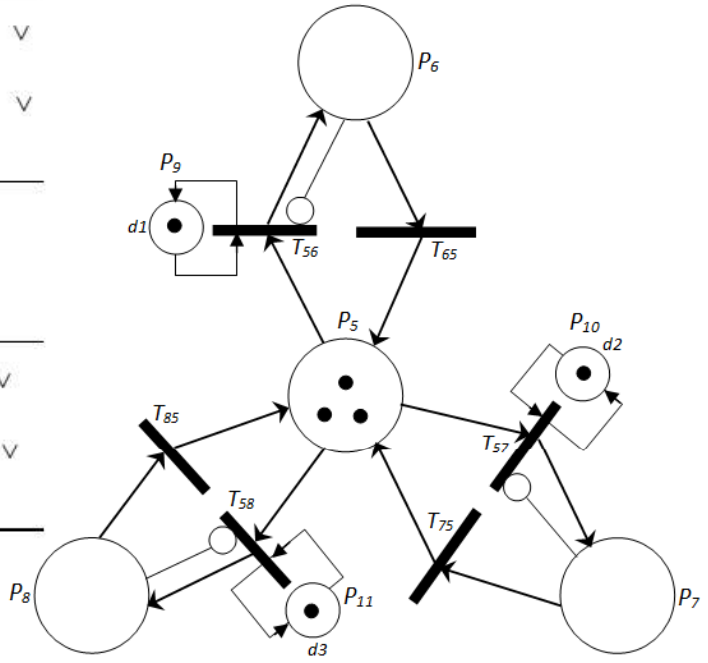
Transitions	Designations
T_{12}	$\alpha = 1 \ \wedge \ (0 < i_{ref} \leq \frac{1}{3} i_{\max}) \ \wedge \ [i_s \leq (i_{ref} - \delta)]$
T_{21}	$\alpha = 2 \ \wedge \ (0 < i_{ref} \leq \frac{1}{3} i_{\max}) \ \wedge \ [i_s \geq (i_{ref} + \delta)]$
T_{13}	$\alpha = 1 \ \wedge \ (\frac{1}{3} i_{\max} < i_{ref} \leq \frac{2}{3} i_{\max}) \ \wedge \ [i_s \leq (i_{ref} - \delta)]$
T_{31}	$\alpha = 3 \ \wedge \ (0 < i_{ref} \leq \frac{1}{3} i_{\max}) \ \wedge \ [i_s \geq (i_{ref} + \delta)]$
T_{14}	$\alpha = 1 \ \wedge \ (\frac{2}{3} < i_{ref} \leq i_{\max}) \ \wedge \ [i_s \leq (i_{ref} - \delta)]$
T_{41}	$\alpha = 4 \ \wedge \ (0 < i_{ref} \leq \frac{1}{3} i_{\max}) \ \wedge \ [i_s \geq (i_{ref} + \delta)]$
T_{23}	$\alpha = 2 \ \wedge \ (\frac{1}{3} i_{\max} < i_{ref} \leq \frac{2}{3} i_{\max}) \ \wedge \ [i_s \leq (i_{ref} - \delta)]$
T_{32}	$\alpha = 3 \ \wedge \ (\frac{1}{3} i_{\max} < i_{ref} \leq \frac{2}{3} i_{\max}) \ \wedge \ [i_s \geq (i_{ref} + \delta)]$
T_{24}	$\alpha = 2 \ \wedge \ (\frac{2}{3} i_{\max} < i_{ref} \leq i_{\max}) \ \wedge \ [i_s \leq (i_{ref} - \delta)]$
T_{42}	$\alpha = 4 \ \wedge \ (\frac{1}{3} i_{\max} < i_{ref} \leq \frac{2}{3} i_{\max}) \ \wedge \ [i_s \geq (i_{ref} + \delta)]$
T_{34}	$\alpha = 3 \ \wedge \ (\frac{2}{3} i_{\max} < i_{ref} \leq i_{\max}) \ \wedge \ [i_s \leq (i_{ref} - \delta)]$
T_{43}	$\alpha = 4 \ \wedge \ (\frac{2}{3} i_{\max} < i_{ref} \leq i_{\max}) \ \wedge \ [i_s \geq (i_{ref} + \delta)]$

Performance



Hybrid control by Petri Nets

Transitions	Designations
T_{56}	$\alpha = 1 \wedge \begin{bmatrix} (v_{c_1} > v_{ref_1}) \wedge (v_{c_2} < v_{ref_2}) \wedge (e_1 > e_2) \vee \\ (v_{c_1} > v_{ref_1}) \wedge (v_{c_2} > v_{ref_2}) \end{bmatrix} \wedge [(e_1 \geq \varepsilon_1) \vee (e_2 \geq \varepsilon_2)] \vee$ $\alpha = 2 \wedge \begin{bmatrix} (v_{c_1} < v_{ref_1}) \wedge (v_{c_2} > v_{ref_2}) \wedge (e_1 < e_2) \vee \\ (v_{c_1} > v_{ref_1}) \wedge (v_{c_2} < v_{ref_2}) \vee \\ (v_{c_1} > v_{ref_1}) \wedge (v_{c_2} > v_{ref_2}) \end{bmatrix} \wedge [(e_1 \geq \varepsilon_1) \vee (e_2 \geq \varepsilon_2)] \vee$ $\alpha = 3$
T_{57}	$\alpha = 1 \wedge [(v_{c_1} < v_{ref_1}) \wedge (v_{c_2} > v_{ref_2})] \wedge [(e_1 \geq \varepsilon_1) \vee (e_2 \geq \varepsilon_2)] \vee$ $\alpha = 2 \wedge \begin{bmatrix} (v_{c_1} < v_{ref_1}) \wedge (v_{c_2} < v_{ref_2}) \vee \\ (v_{c_1} < v_{ref_1}) \wedge (v_{c_2} > v_{ref_2}) \vee \\ (v_{c_1} > v_{ref_1}) \wedge (v_{c_2} > v_{ref_2}) \end{bmatrix} \wedge [(e_1 \geq \varepsilon_1) \vee (e_2 \geq \varepsilon_2)] \vee$ $\alpha = 3$
T_{58}	$\alpha = 1 \wedge \begin{bmatrix} (v_{c_1} < v_{ref_1}) \wedge (v_{c_2} < v_{ref_2}) \vee \\ (v_{c_1} > v_{ref_1}) \wedge (v_{c_2} < v_{ref_2}) \wedge (e_1 < e_2) \end{bmatrix} \wedge [(e_1 \geq \varepsilon_1) \vee (e_2 \geq \varepsilon_2)] \vee$ $\alpha = 2 \wedge \begin{bmatrix} (v_{c_1} < v_{ref_1}) \wedge (v_{c_2} < v_{ref_2}) \vee \\ (v_{c_1} < v_{ref_1}) \wedge (v_{c_2} > v_{ref_2}) \wedge (e_1 > e_2) \vee \\ (v_{c_1} > v_{ref_1}) \wedge (v_{c_2} < v_{ref_2}) \end{bmatrix} \wedge [(e_1 \geq \varepsilon_1) \vee (e_2 \geq \varepsilon_2)] \vee$ $\alpha = 3$



Petri Net to get the capacitor voltage balancing

Places	Designations
P_5	Initial State
P_6	State of the switch in the first switching cell
P_7	State of the switch in the second switching cell
P_8	State of the switch in the third switching cell
P_9, P_{10}, P_{11}	Timed places to assign the authorized time between two switching of a switch, d_1, d_2, d_3

Performance

1. The selected state will reduce the voltage error in each capacitor or at least this error will remain unchanged.
2. If there are two or more selectable states according to the first point, the state that compensate the higher number of capacitors will be set.
3. If there are two or more selectable states according to the second point, the state that reduces the error, in that capacitor with greatest deviation on its voltage reference, will be selected.

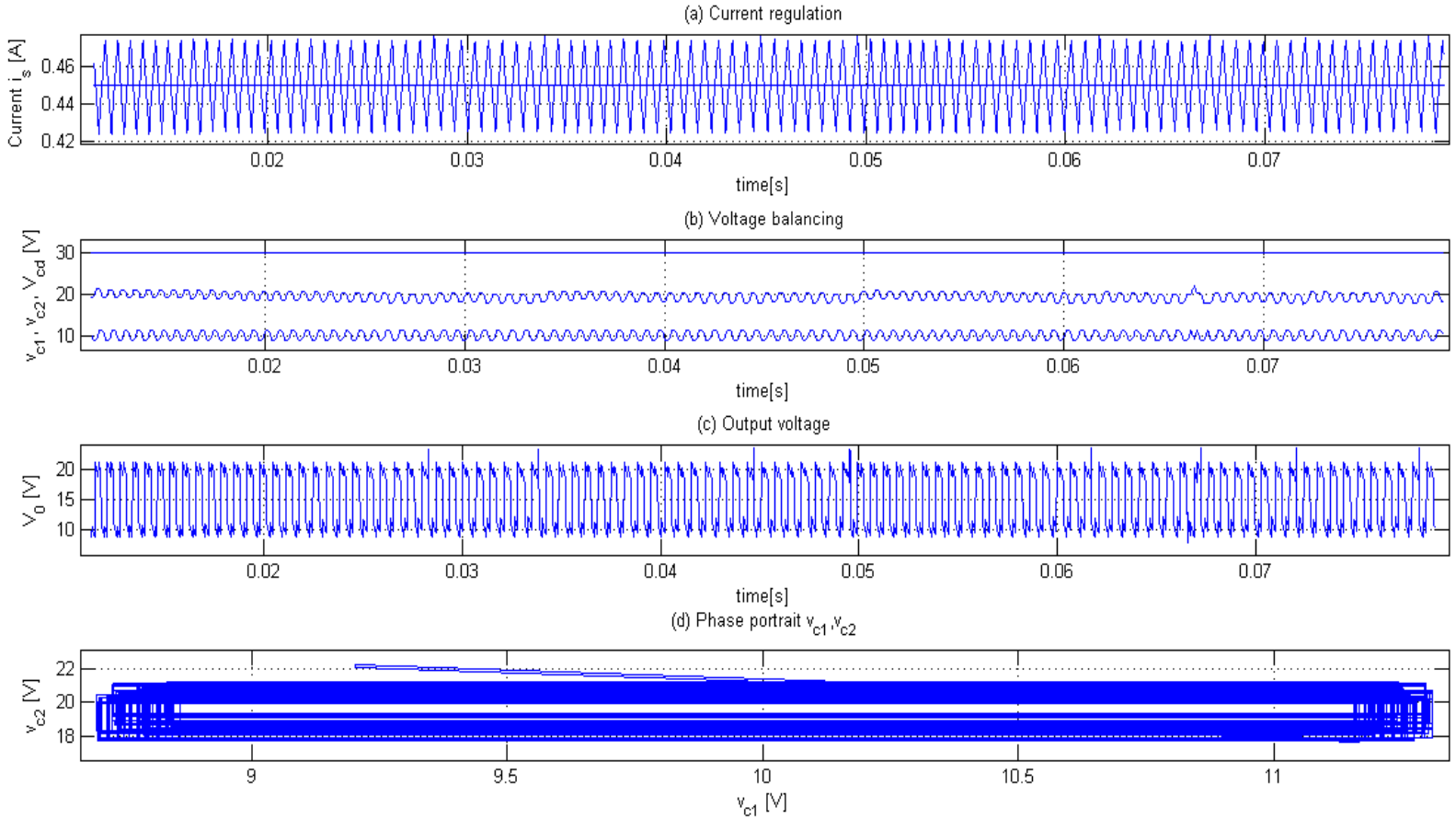
Simulation Results

Parameters

$$R = 33\Omega,\ L = 32mH,\ C_1 = C_2 = 33\mu F$$

$$vc_1(0) = vc_2(0) = 0V,\ V_{cd} = 30V,\ d_1 = d_2 = d_3 = \frac{1}{f_c} = 2\times10^{-5}s$$

$$\delta = \pm 0.05 \times i_{ref},\ \varepsilon_1 = 1.5V,\ \varepsilon_2 = 2V,\ i_{ref} = 0.45A$$



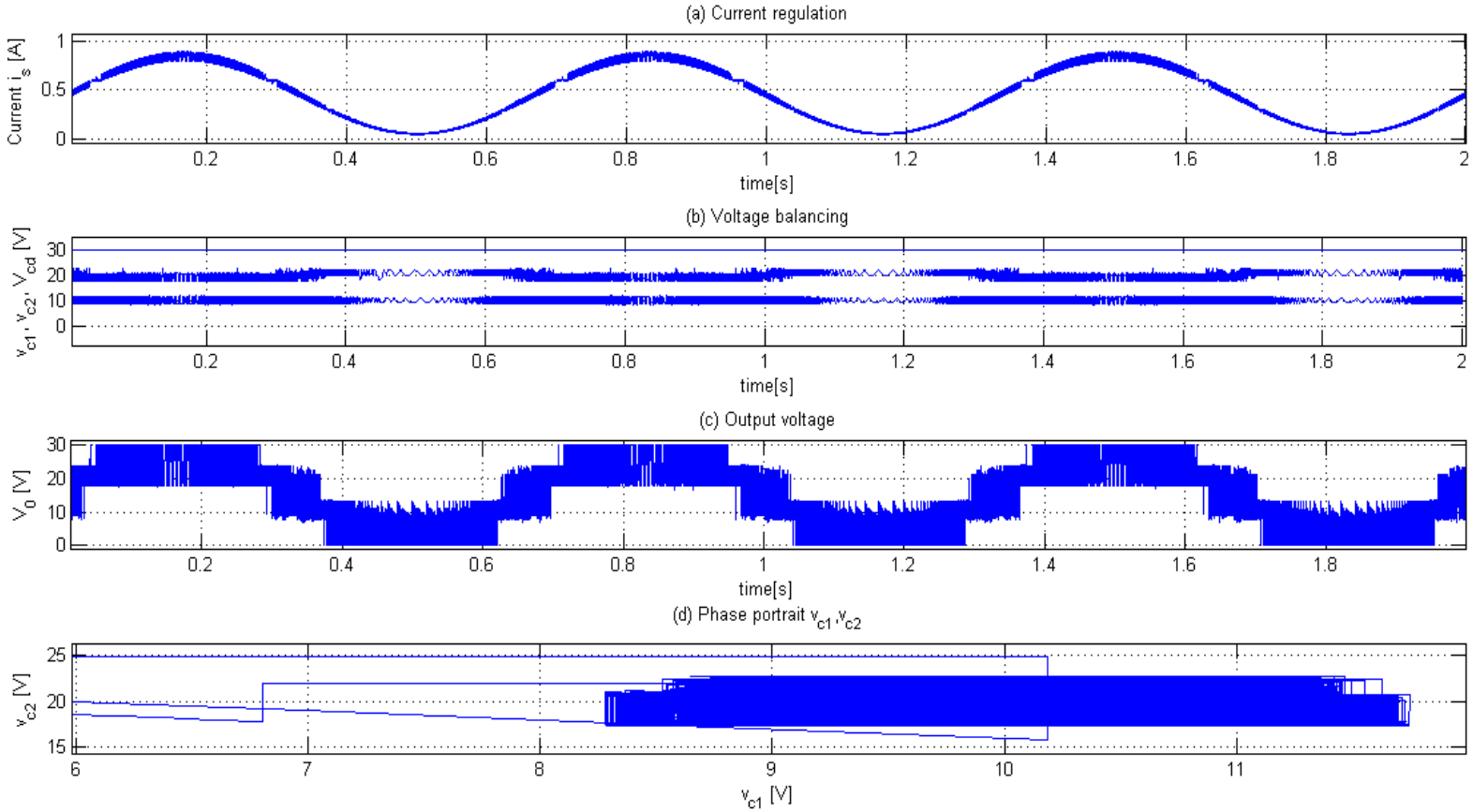
Simulation Results

Parameters

$R = 33\Omega,\ L = 32mH,\ C_1 = C_2 = 33\mu F$

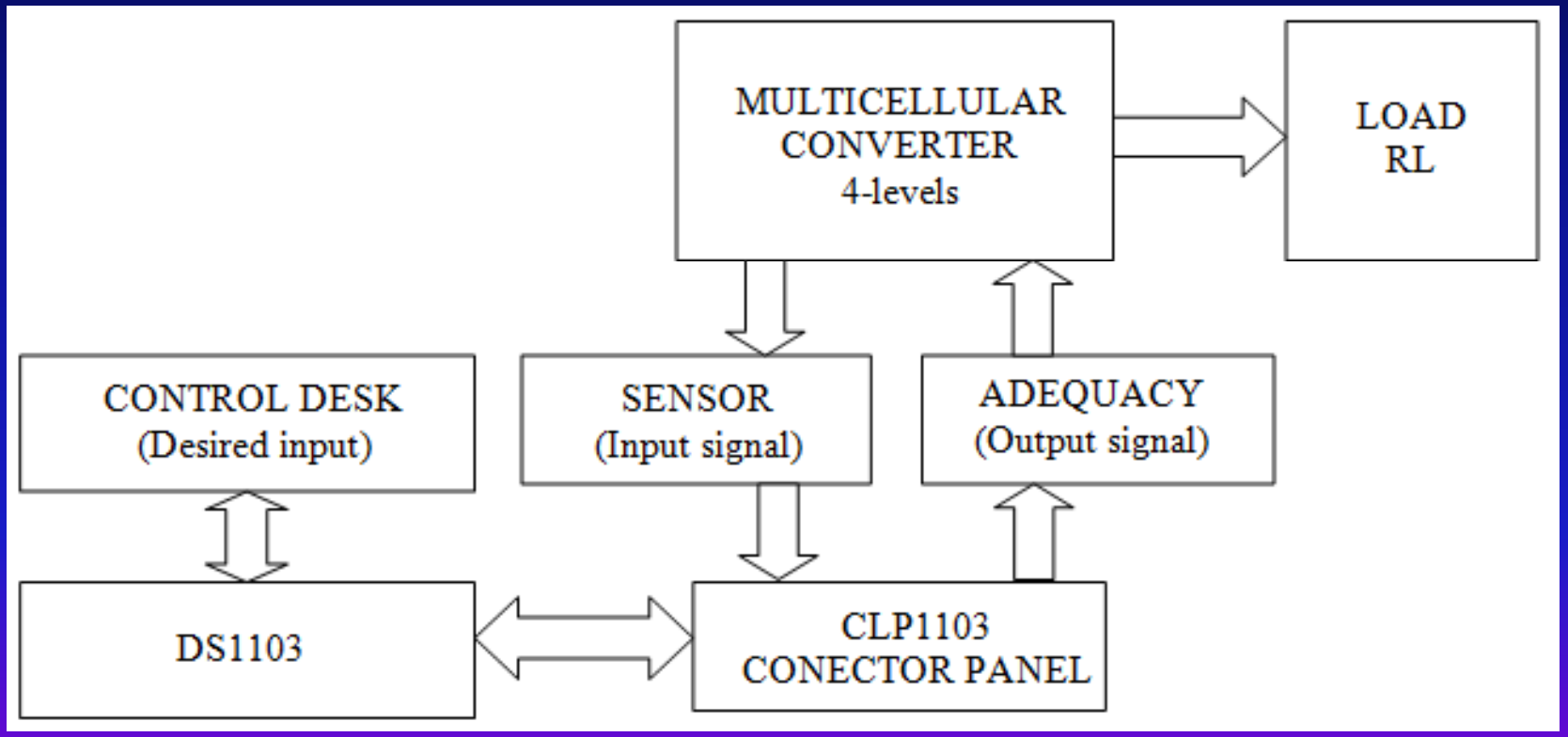
$vc_1(0) = vc_2(0) = 0V,\ V_{cd} = 30V,\ d_1 = d_2 = d_3 = \frac{1}{f_c} = 2\times10^{-5}s$

$\delta = \pm 0.05 \times i_{ref},\ i_{ref} = 0.4A,\ offset = 0.45,\ freq = 1.5Hz$

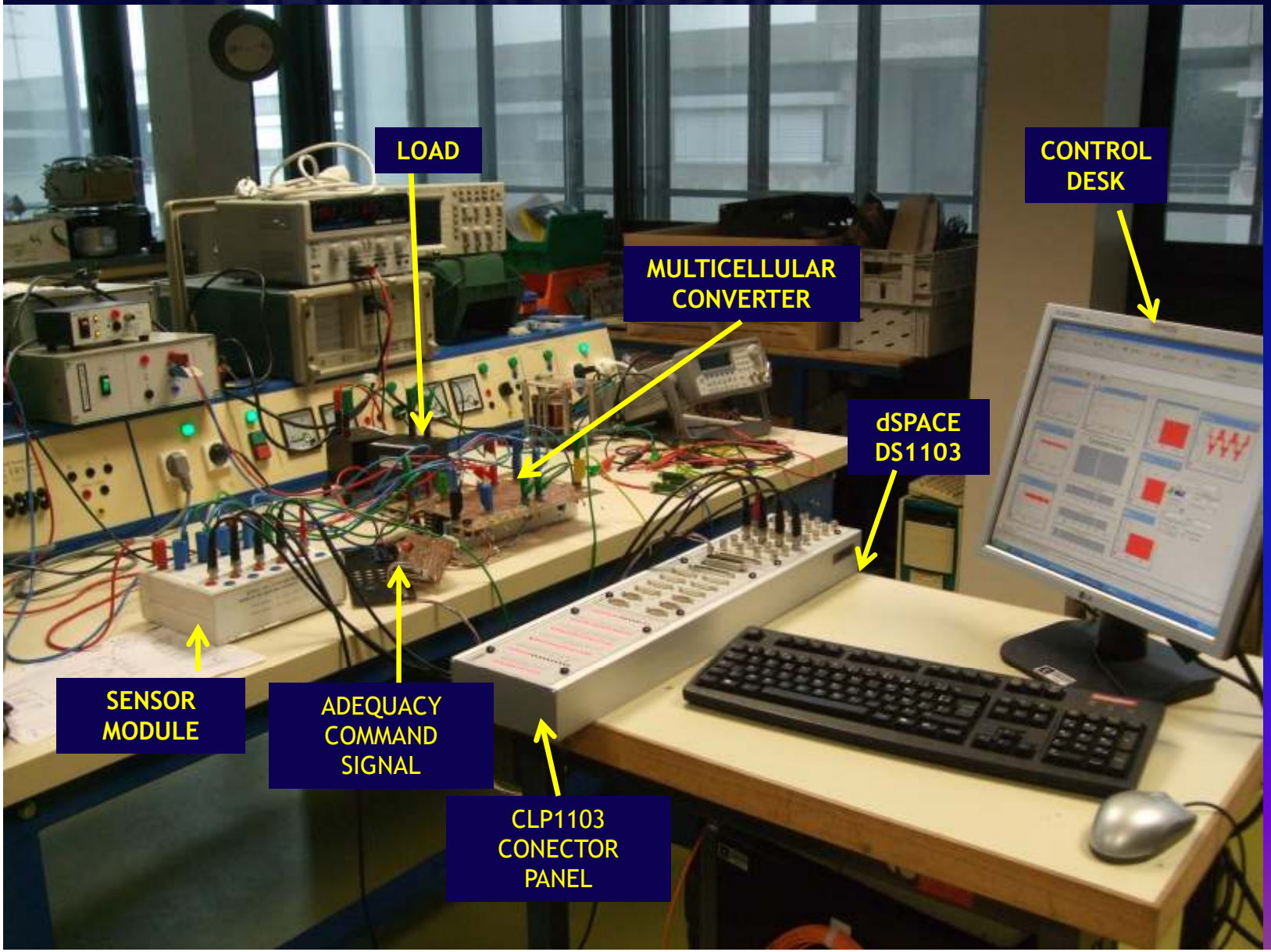


Experimental Results

Control System Diagram



Experimental Results



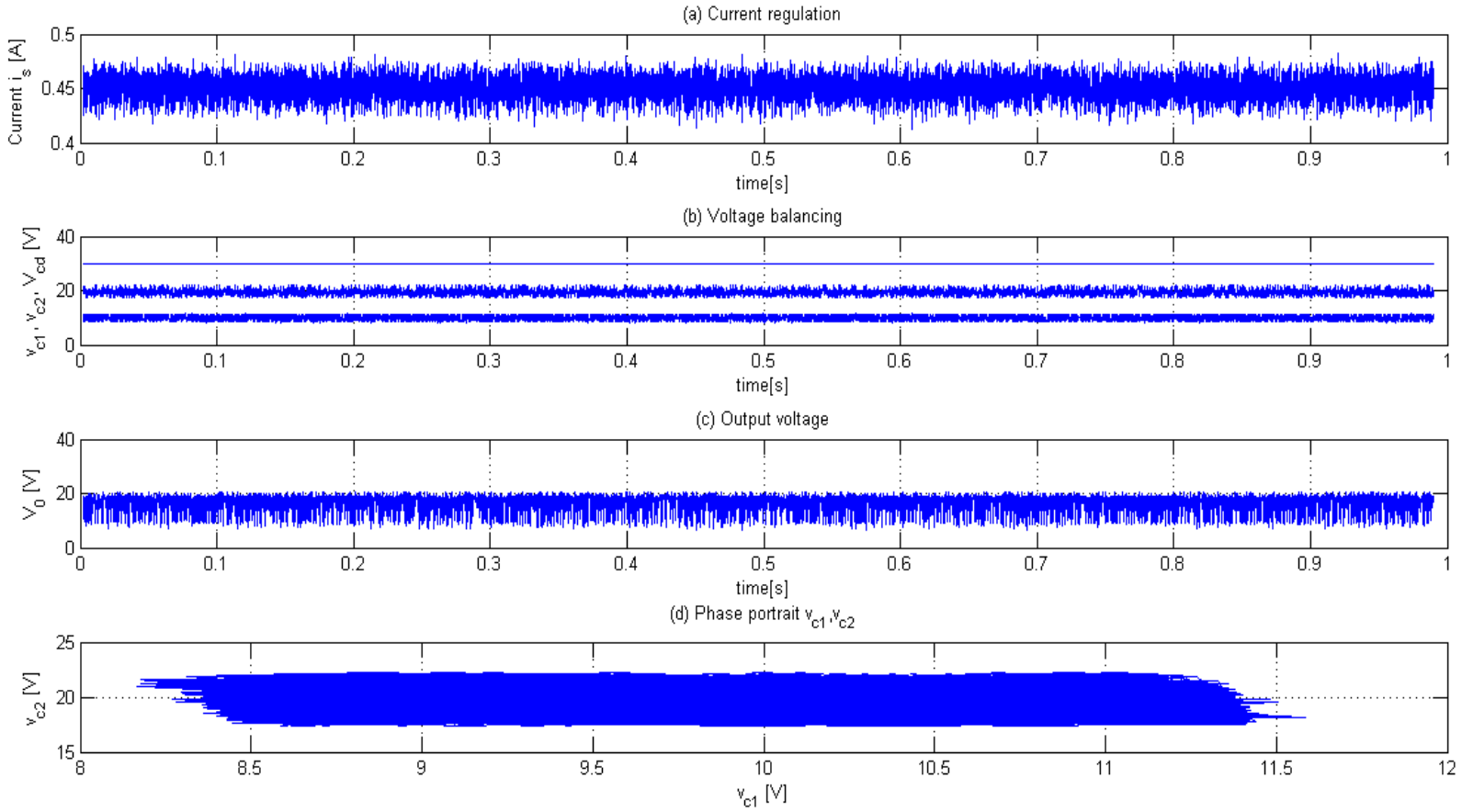
Experimental Results

Parameters

$$R = 33\Omega,\ L = 32mH,\ C_1 = C_2 = 33\mu F$$

$$vc_1(0) = vc_2(0) = 0V,\ V_{cd} = 30V,\ d_1 = d_2 = d_3 = \frac{1}{f_c} = 1.42\times10^{-5}\,s$$

$$\delta = \pm 0.05 \times i_{ref},\ i_{ref} = 0.45A$$



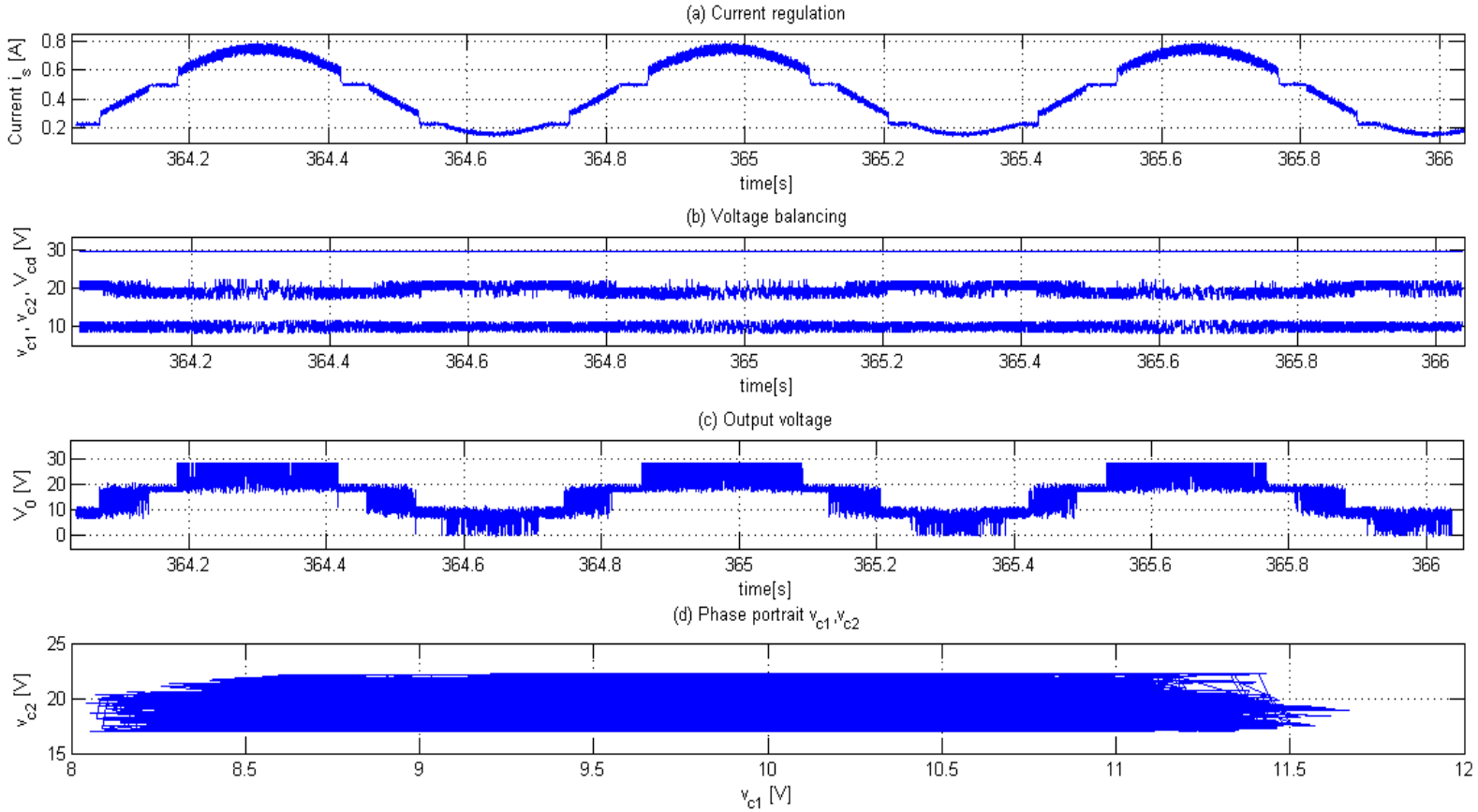
Experimental Results

Parameters

$$R = 33\Omega,\ L = 32mH,\ C_1 = C_2 = 33\mu F$$

$$vc_1(0) = vc_2(0) = 0V,\ V_{cd} = 30V,\ d_1 = d_2 = d_3 = \frac{1}{f_c} = 1.42\times10^{-5}\,s$$

$$\delta = \pm 0.05 \times i_{ref},\ i_{ref} = 0.4A,\ offset = 0.45,\ freq = 1.5Hz$$



Conclusions

- It has been presented an algorithm to control the current and the capacitor voltages in a SMC of 4 levels.
- Its operation is based in two Petri Nets.
  a) Synthesizes a voltage signal according to current reference.
  b) Generates the pulses in function of state of charge in each capacitor and the input reference of voltage.
- Incorporation of Petri Nets as a design tool of control in power electronics systems. Integration of redundancy of switching states in the PWM technique.
- Simulation and experimental results demosntrate the effectiveness of the control strategy.